LISTING OF THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A method for testing a semiconductor memory device, comprising:

a first step of generating n number of first internal addresses including [[an]] a first external address supplied for designating a storage region of data for 1 bit to be written into a storage unit of a semiconductor memory device, in synchronization with a high-speed clock which has a frequency n times that of an external ~~clock (n is a natural number)~~ clock, n being a natural number, and is synchronized with the external clock, generating n bits of internal write data corresponding to n number of the internal addresses in synchronization with the high-speed clock and writing the generated internal write data into the storage unit, a first data generating method of generating the n bits of the internal write data being consecutively generating n number of values of "1"; and

a second step of latching [[an]] a second external address supplied for designating a storage region of data for 1 bit to be read from the storage unit, generating n number of second internal addresses including the second external address in synchronization with the high-speed clock, reading n bits of internal read data corresponding to n number of the second internal addresses from the storage unit in synchronization with the high-speed clock and outputting the internal read data corresponding to the second internal address, which coincides with the latched second external address, out of n number of the internal addresses.

2. (Currently Amended) The method for testing a semiconductor memory device, according to claim 1, wherein

in the second step, 1 bit of the internal read data read from the storage unit in accordance with one of n number of the internal addresses, which coincides with the latched second external address and is synchronized with the high-speed clock, is outputted.

3. **(Currently Amended)** The method for testing a semiconductor memory device, according to claim 1, wherein

n number of the first and second internal addresses are generated by use of any one of a first address generating method of generating the first and second internal addresses by sequentially increasing an address of the first and second external ~~address~~ addresses, respectively, a second address generating method of generating the first and second internal addresses by sequentially decreasing the address of the first and second external ~~address~~ addresses, respectively, and a third address generating method of generating the first and second internal addresses within a range which includes the first and second external ~~address~~ addresses, respectively, and is separated by n.

4. **(Currently Amended)** The method for testing a semiconductor memory device, according to claim 1, wherein

additional data generating methods of generating the n bits of the internal write data are ~~generated by use of any one of a first data generating method of consecutively generating n number of values of "1",~~ a second data generating method of consecutively generating n number of values of "0", a third data generating method of alternately repeating the values "1" and "0" in this order and a fourth data generating method of alternately repeating the values "0" and "1" in this order.

5. **(Currently Amended)** A test circuit for a semiconductor memory device, comprising:

a high-speed clock generating circuit which generates a high-speed clock which has a frequency n times that of an external ~~clock (n is a natural number)~~ clock, n being a natural number, and is synchronized with the external clock;

a high-speed address generating circuit which generates, in synchronization with the high-speed clock, n number of first internal addresses including a first external address supplied for designating a storage region of data for 1 bit to be written into a storage unit of a semiconductor memory device, latches a second external address supplied for designating a storage region of

data for 1 bit to be read from the storage unit, outputs the second external address as a latch address and generates n number of second internal addresses including the second external address in synchronization with the high-speed clock; and

a high-speed data generating circuit which generates n bits of internal write data corresponding to n number of the first internal addresses in synchronization with the high-speed clock, a first data generating method of generating the n bits of the internal write data being consecutively generating n number of values of "1", and supplies the internal write data to the storage unit and outputs internal read data corresponding to one of n number of the second internal addresses, which coincides with the latch address, out of n bits of the internal read data read from the storage unit in synchronization with the high-speed clock.

6. (Original) The test circuit for a semiconductor memory device, according to claim 5, wherein the high-speed data generating circuit outputs 1 bit of the internal read data read from the storage unit in accordance with one of n number of the internal addresses, which coincides with the latch address and is synchronized with the high-speed clock.

7. (Currently Amended) The test circuit for a semiconductor memory device, according to claim 5, wherein the high-speed address generating circuit includes any one of first address generating means for generating the internal addresses by sequentially increasing an address of the external address, second address generating means for generating the internal addresses by sequentially decreasing the address of the external address and third address generating means for generating the internal addresses within a range which includes the external address and is separated by [[n]] n.

8. (Currently Amended) The test circuit for a semiconductor memory device, according to claim 5, wherein ~~the high-speed data generating circuit generates~~ additional data generating methods of generating the n bits of the internal write data ~~by use of any one of a first data generating method of consecutively generating n number of values of "1",~~ are a second data generating method of consecutively generating n number of values of "0", a third data generating

method of alternately repeating the values "1" and "0" in this order and a fourth data generating method of alternately repeating the values "0" and "1" in this order.

9. **(Original)** The test circuit for a semiconductor memory device, according to claim 5, wherein

the high-speed address generating circuit includes an external address fetch/latch circuit and an internal address generating circuit,

the external address fetch/latch circuit fetches the external address, latches the external address to be supplied to the high-speed data generating circuit as a latch address and transfers the fetched external address to the internal address generating circuit, and

the internal address generating circuit generates, in synchronization with the high-speed clock, n number of the internal addresses including the external address supplied from the external address fetch/latch circuit.